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floating. This causes Fowler-Nordheim tunnelling of electrons from the floating gate to the substrate through the thin gate oxide near the source.

As previously stated, drain disturbance occurs in adjacent cells during programming of a selected cell due to the fact that each of the transistors 14 have their drains commonly coupled to a single column line 12. For example, if cell 14a is being programmed, then the drain of cell 14b is also at a potential of approximately 7 volts. Due to the fact that the control gate 15b is grounded during the programming of cell 14a, an erase-like condition is developed in cell 14b. That is, electrons residing on the floating gate 11b are attracted to the drain region by the relatively high potential present on column line 12a. If the gate oxide is relatively thin near the drain (e.g., ~100 Å) then Fowler-Nordheim tunnelling of electrons may occur.

As is apparent to one skilled in the art, this type of disturbance to the programming state of adjacent cell 14b is disadvantageous. To alleviate this problem, the present invention provides for a thicker gate oxide near the drain region to reduce drain disturbance while retaining a relatively thin gate oxide near the source to avoid interfering with the erase performance of individual cells.

In accordance with the method of the present invention the preferred embodiment of the invented process is readily compatible with conventional EPROM and EEPROM process flows. In other words, the presently invented method for forming a two-tiered tunnel oxide

implanted silicon. In the preferred embodiment, argon is implanted at an energy of 40 KeV and at a dose of approximately 4.0×10^{14} atoms per square centimeter.

Other species are also effective in enhancing the thermal oxidation rate. Antimony, argon, arsenic, and boron, or any one of the group III-IV dopants, have proven effective for enhancing oxidation rates in silicon.

With reference to FIG. 5, after the argon implant has been completed, photoresist layer 27 is stripped and thermal oxidation of the channel may proceed. The thermal oxidation takes place in a furnace at a temperature of around 950° C. for a period of approximately 10 minutes in a dry O₂ atmosphere. During the gate oxide growth, the oxidation rate over channel region 25b is higher than that associated with channel region 25a due to the previous ion implant damage to the lattice. The result of this oxidation is shown in FIG. 5 wherein oxide 31 above region 25b is comparatively thicker than oxide 30 over region 25a. Preferably, oxide 31 is grown approximately 120 Å thick and oxide 30 is grown approximately 90 Å thick.

Following growth of the two-tiered tunnel oxide structure, the fabrication of the device may be completed according to any one of a number of well-known fabrication techniques. Usually, a polysilicon layer is first deposited over the surface of the device followed by an insulative material—most often silicon dioxide. A second layer of polysilicon is then deposited over the silicon dioxide and the entire structure is etched so that